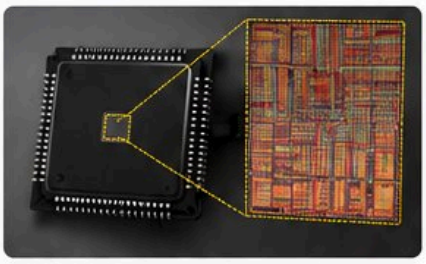
INTRODUCTION TO VLSI

(Very Large Scale Integration)

VLSI is the process of integrating hundreds of thousands to millions (or more) of transistors on a single semiconductor chip to realize complex electronic systems.

1. What is VLSI?

- VLSI stands for Very Large Scale Integration.
- It involves fabricating an entire electronic system on a single IC chip.
- It is the technology behind modern microprocessors, memories, DSPs, FPGAs, ASICs, SoCs and more.
- It combines millions/billions of transistors with interconnections on a tiny silicon area.



A modern VLSI chip (microprocessor die)

2. Evolution of Integration

Era	Year (approx.)	Integration Level	Examples
SSI	1960s	< 10 gates	Simple gates, flip-flops
MSI	1970s	10 – 100 gates	Counters, encoders
LSI	1980s	100 – 10,000 gates	Microprocessors, memory chips
VLSI	1990s	10,000 – 1 million gates	ASICs, DSPs
ULSI	2000s and beyond	> 1 million gates	SoC, GPUs, AI chips

Increasing integration, speed, functionality and density

3. Why VLSI?

- ✓ High performance and speed
- ✓ Very small size and weight
- ✓ Low power consumption
- ✓ High reliability
- ✓ Mass production → Low cost
- ✓ More functionality
- ✓ Enables portability and miniaturization

4. VLSI Design Abstraction Levels

- **System Level** — Algorithm, architecture, specifications
- **RTL (Register Transfer Level)** — HDL description (Verilog/VHDL)
- **Logic Level** — Logic gates, Boolean operations
- **Circuit Level** — Transistors, resistors, capacitors
- **Physical Level** — Layout, mask, fabrication

Increasing Detail

5. Basic VLSI Design Flow

1. **Specification** — Define functionality, performance, power, area, technology.
2. **RTL Design** — Design using HDL (Verilog/VHDL).
3. **Logic Synthesis** — Convert RTL to gate-level netlist.
4. **Verification** — Functional and timing verification, simulation.
5. **Physical Design** — Floorplanning, placement, routing, clock tree synthesis.
6. **Sign-off** — Timing, power, DRC, LVS checks.
7. **Fabrication** — Mask generation and wafer fabrication.
8. **Testing** — Wafer probing, packaging and testing.
9. **Product** — Tinalg, power, DRC, LVS checks.

6. VLSI Design Styles

- **Full Custom Design**
  - Best performance and lowest power
  - Highest design time and cost
- **Semi-Custom Design**
  - Uses standard cells and pre-designed blocks
  - Faster design, moderate cost
- **Programmable Logic Design**
  - Uses PLDs, FPGAs
  - Reconfigurable, flexible

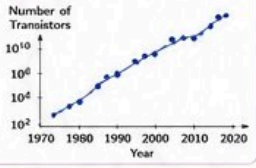
7. Key VLSI Metrics

- **Area** : Silicon area occupied by the design.
- **Speed (Performance)** : Maximum operating frequency or minimum delay.
- **Power** : Total power consumption (dynamic + static).
- **Power-Delay Product** : Important for energy efficiency.
- **Yield** : Ratio of good chips to total chips fabricated.

8. VLSI Technology Scaling (Moore's Law)

The number of transistors on a chip doubles approximately every 18–24 months, leading to:

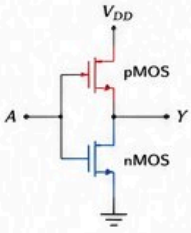
- Higher density
- Better performance
- Lower power
- Lower cost per function



9. Basic CMOS Technology

CMOS (Complementary Metal Oxide Semiconductor) is the most widely used VLSI technology.

CMOS Inverter



When A = 0
pMOS ON, nMOS OFF
Y = 1

When A = 1
pMOS OFF, nMOS ON
Y = 0

CMOS offers: Low power, High noise margin, High density, Scalability.

10. Applications of VLSI

- Microprocessors and Microcontrollers
- Memory Chips (SRAM, DRAM, Flash)
- Digital Signal Processors (DSP)
- Communication Systems (wireless, RF)
- Consumer Electronics (mobiles, TVs)
- Automotive and Industrial Electronics
- AI/ML Accelerators and SoCs

11. Challenges in VLSI

- ⚠ Heat dissipation
- ⚠ Power density
- ⚠ Interconnect delay
- ⚠ Process variations
- ⚠ Design complexity
- ⚠ Reliability and aging
- ⚠ Scaling limitations

12. VLSI Design Tools (Examples)

- HDL Tools : ModelSim, Vivado, Quartus
- Synthesis Tools : Synopsys Design Compiler
- Physical Design : Cadence Innovus
- Verification : Questa, VCS
- Simulation : SPICE, HSPICE
- Layout : Cadence Virtuoso

13. Summary

VLSI technology makes it possible to integrate a complete system on a single chip by combining:

- ✓ Advanced semiconductor fabrication
- ✓ Sophisticated design methodologies
- ✓ Powerful CAD tools

It continues to drive the progress of modern electronics and revolutionize the world.

14. Glossary

VLSI	Very Large Scale Integration	ASIC	Application Specific Integrated Circuit	DRC	Design Rule Check
IC	Integrated Circuit	FPGA	Field Programmable Gate Array	LVS	Layout Versus Schematic
RTL	Register Transfer Level	SoC	System on Chip	PDK	Process Design Kit
HDL	Hardware Description Language	CMOS	Complementary Metal Oxide Semiconductor		

> "VLSI is the art of designing billions of transistors to work as one intelligent system."

MOSFET

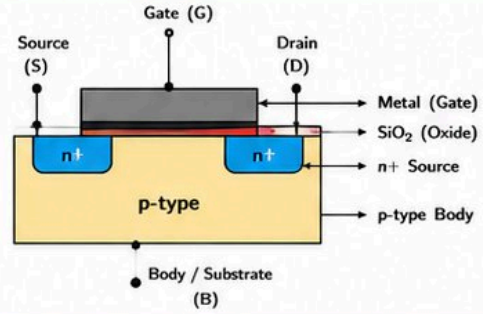
Metal–Oxide–Semiconductor Field–Effect Transistor

A MOSFET is a voltage-controlled unipolar device used for amplification and switching. It has very high input impedance, low power consumption and high speed. It is the most widely used transistor in VLSI and modern electronics.

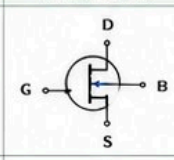
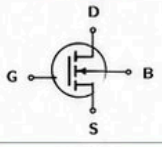
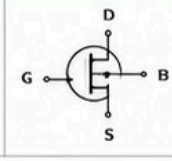
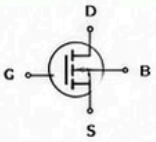
1. What is MOSFET?

- A majority carrier device (unipolar).
- Consists of Metal–Oxide–Semiconductor structure.
- Gate voltage controls the current between Drain and Source.
- Very high input impedance → almost no gate current in steady state.
- Available in two types:
  - Enhancement Mode
  - Depletion Mode

2. MOSFET Structure (n-Channel)



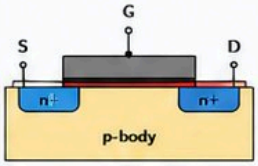
3. Types of MOSFET

	Enhancement Mode (Normally OFF)	Depletion Mode (Normally ON)	Symbol Convention
n-Channel			Arrow shows direction of conventional current when device is ON. n-Channel: arrow points IN p-Channel: arrow points OUT
p-Channel			

4. Operation (n-Channel Enhancement MOSFET)

(a) Cut-off Region (OFF)

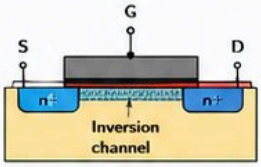
$V_{GS} < V_{TH}$



- No inversion channel.
- $I_D \approx 0$ (only leakage).
- Transistor is OFF.

(b) Linear / Triode Region (ON)

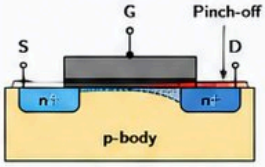
$V_{GS} > V_{TH}$, $0 < V_{DS} < V_{GS} - V_{TH}$



- Inversion channel formed.
- Behaves like a voltage controlled resistor.
- I_D increases with V_{DS}.

(c) Saturation Region (Active)

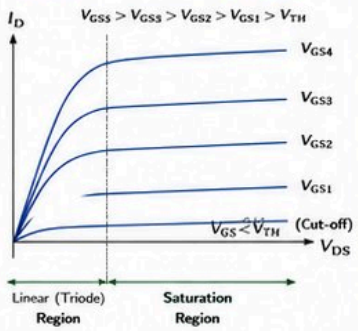
$V_{GS} > V_{TH}$, $V_{DS} \geq V_{GS} - V_{TH}$



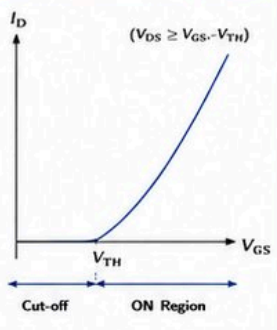
- Channel pinch-off near drain.
- I_D becomes almost constant (independent of V_{DS}).
- Used for amplification.

5. V–I Characteristics (n-Channel Enhancement)

(a) Output Characteristics (I_D vs V_{DS})



(b) Transfer Characteristics (I_D vs V_{GS})



6. Important Equations (n-Channel Enhancement)

(a) Linear / Triode Region

$(0 < V_{DS} < V_{GS} - V_{TH})$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

(b) Saturation Region

$(V_{DS} \geq V_{GS} - V_{TH})$

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

Where,

- μ_n = Electron mobility
- C_{ox} = Oxide capacitance per unit area
- W = Channel width
- L = Channel length
- V_{TH} = Threshold voltage
- λ = Channel length modulation parameter

7. Threshold Voltage (V_{TH})

- Minimum gate-to-source voltage required to form an inversion channel.
- Depends on doping, oxide thickness, and work function.
- For n-channel:

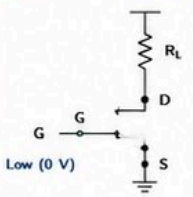
$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\epsilon_s N_A 2\phi_F}}{C_{ox}}$$

Where,

- V_{FB} = Flat-band voltage
- ϕ_F = Fermi potential
- N_A = Substrate doping
- q = Electron charge
- ϵ_s = Semiconductor permittivity
- C_{ox} = Oxide capacitance per unit area

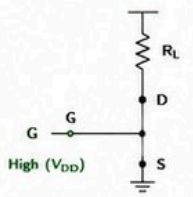
8. MOSFET as a Switch

(a) OFF State ($V_{GS} < V_{TH}$)



$I_D \approx 0$
Open Switch

(b) ON State ($V_{GS} > V_{TH}$)



I_D is large
Closed Switch

9. Comparison: MOSFET vs BJT

Parameter	MOSFET	BJT
Type	Unipolar	Bipolar
Control	Voltage Controlled	Current Controlled
Input Impedance	Very High	Low to Moderate
Input Current	~ 0 (Steady State)	Requires Base Current
Power Consumption	Low	Higher
Speed	High	Lower
Thermal Stability	Good	Poorer
Applications	VLSI, Switching, Analog, Power	Amplifiers, Linear Applications

12. Applications

- Digital ICs (CMOS Logic Gates, Memories)
- Power Switching (DC–DC converters, MOSFET drivers)
- Analog Amplifiers and Filters
- Motor Control and Robotics
- RF Circuits and Communication
- VLSI and SoC Design

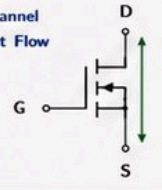
11. Key Points

- ✓ MOSFET is a voltage-controlled device with very high input impedance.
- ✓ n-Channel conducts when $V_{GS} > V_{TH}$; p-Channel conducts when $V_{SG} > |V_{TH}|$.
- ✓ Used in both analog (amplifiers) and digital (switches) circuits.
- ✓ Foundation device for CMOS technology in VLSI.

12. Common Terminology

- **Gate (G)** : Control terminal
- **Drain (D)** : Output terminal
- **Source (S)** : Reference terminal
- **Body / Bulk (B)** : Substrate terminal
- V_{GS} : Gate-to-Source Voltage
- I_D : Drain Current

N-Channel Current Flow



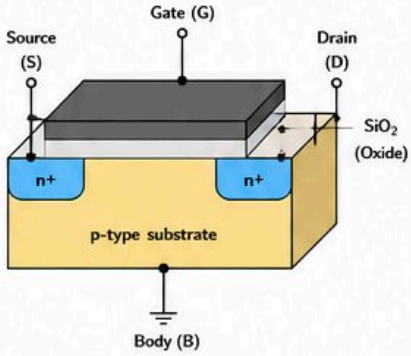
THRESHOLD VOLTAGE (V_{TH}) AND ITS DERIVATION

1. Introduction

Threshold voltage (V_{TH}) is the minimum gate-to-source voltage required to create a strong inversion layer at the surface of the semiconductor, forming a conducting channel between source and drain.

Below V_{TH}: No channel

Above V_{TH}: Inversion channel forms and current flows.

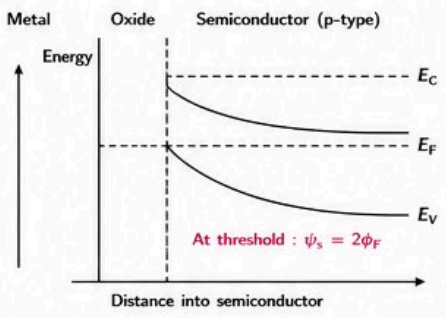


2. Threshold Condition (Strong Inversion)

At threshold ($V_{GS} = V_{TH}$):

The surface potential at the semiconductor-oxide interface (ψ_s) equals twice the Fermi potential (ϕ_F).

$$\psi_s = 2\phi_F$$



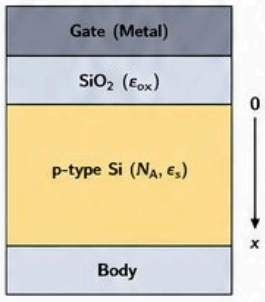
3. Preliminaries

- p-type substrate with acceptor doping N_A
- Oxide thickness = t_{ox}, permittivity = ε_{ox}
- Semiconductor permittivity = ε_s
- Fermi potential (ϕ_F)

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

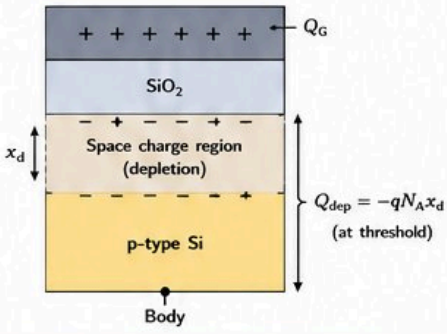
where, n_i = intrinsic carrier concentration

MOS Capacitor Cross-section



4. Charge Distribution at Threshold

- Inversion charge at the surface (sheet charge):
  $Q_{inv} = -qN_A x_d$
- Depletion charge in the semiconductor:
  $Q_{dep} = -qN_A x_d$
- At threshold, total negative charge in the semiconductor is balanced by positive charge on the gate (Q_G).



5. Derivation of Threshold Voltage

Step 1: Depletion Width at Threshold

From Poisson's equation in depletion region,

$$x_d = \sqrt{\frac{2\varepsilon_s \psi_s}{qN_A}}$$

At threshold, $\psi_s = 2\phi_F$

$$x_d = \sqrt{\frac{4\varepsilon_s \phi_F}{qN_A}}$$

Step 2: Maximum Depletion Charge

$$Q_{dep,max} = -qN_A x_d$$

$$= -qN_A \sqrt{\frac{4\varepsilon_s \phi_F}{qN_A}}$$

$$Q_{dep,max} = -\sqrt{4\varepsilon_s qN_A \phi_F}$$

Step 3: Gate Voltage Components

The gate voltage at threshold is used up in:

- Flat-band voltage (V_{FB})
- Voltage drop across oxide (V_{ox})
- Surface potential ($\psi_s = 2\phi_F$)

$$V_{TH} = V_{FB} + V_{ox} + 2\phi_F$$

Step 4: Oxide Voltage Drop

From Gauss law (charge balance),

$$C_{ox}\,(V_{ox}) = -\,Q_{dep,max}$$

$$V_{ox} = -\frac{Q_{dep,max}}{C_{ox}}$$

where, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

Step 5: Final Expression for Threshold Voltage

$$V_{TH} = V_{FB} + 2\phi_F + \frac{|Q_{dep,max}|}{C_{ox}} \Rightarrow \boxed{V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_s qN_A \phi_F}}{C_{ox}}}$$

This is the threshold voltage of an n-channel enhancement MOSFET.

6. Flat-Band Voltage (V_{FB})

Defined as the gate voltage that makes the bands flat ($\psi_s = 0$).

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}}$$

where,

- $\phi_{ms} = \phi_m - \phi_s$ (metal–semiconductor work function difference)
- Q_f = fixed oxide charge per unit area (positive if +ve charge in oxide)

7. Fermi Potential (ϕ_F)

It is the potential difference between intrinsic Fermi level and the Fermi level in the semiconductor.

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

At 300 K ($kT/q \approx 25.9$ mV):

$$\phi_F\ (\text{V}) = 0.0259 \ln\left(\frac{N_A}{n_i}\right)$$

Typically $\phi_F \approx 0.2$ to 0.4 V for usual doping.

8. Final Threshold Voltage Expression

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_s qN_A \phi_F}}{C_{ox}}$$

with

- $V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}}$
- $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$
- $\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$

Dependence

- Increases with N_A ↑
- Increases with t_{ox} ↑
- Decreases with ε_{ox} ↑
- Increases with $|Q_f|$ ↑ (for +ve Q_f)
- Depends on work function difference (ϕ_{ms})

9. n-Channel vs p-Channel

n-Channel (on p-type substrate)

$$V_{THn} = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_s qN_A \phi_F}}{C_{ox}}$$

p-Channel (on n-type substrate)

$$V_{THp} = V_{FB} - 2\phi_F - \frac{\sqrt{4\varepsilon_s qN_D \phi_F}}{C_{ox}}$$

(Sign is negative because majority carriers are holes)

10. Typical Values (Example)

$N_A = 10^{16}$ cm^{-3}
$t_{ox} = 10$ nm
$\varepsilon_{ox} = 3.9\,\varepsilon_0$
$\varepsilon_s = 11.7\,\varepsilon_0$
$\phi_{ms} = 0.1$ V,
$Q_f = 0$

$\Rightarrow$

$\phi_F \approx 0.298$ V
$C_{ox} = \frac{3.9\,\varepsilon_0}{10 \times 10^{-9}} = 3.45 \times 10^{-3}$ F/m^2
$V_{FB} = 0.1$ V
$\Rightarrow V_{TH} \approx 0.58$ V (approx.)

11. Physical Meaning

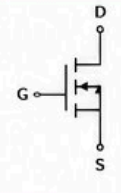
- At $V_{GS} < V_{TH}$: only depletion region exists, no conduction channel.
- At $V_{GS} = V_{TH}$: surface potential = $2\phi_F$, strong inversion just starts.
- At $V_{GS} > V_{TH}$: inversion layer (channel) forms and current flows.

12. Key Points

- ✓ V_{TH} is the minimum gate voltage to create an inversion channel.
- ✓ Increases with substrate doping (N_A for nMOS, N_D for pMOS).
- ✓ Increases with oxide thickness (t_{ox}).
- ✓ Decreases with oxide permittivity (ε_{ox}).
- ✓ Affected by work function difference and fixed oxide charge.

13. Important Application

- Determines the turn-on point of MOSFET.
- Critical in circuit design, power estimation and device scaling in VLSI.

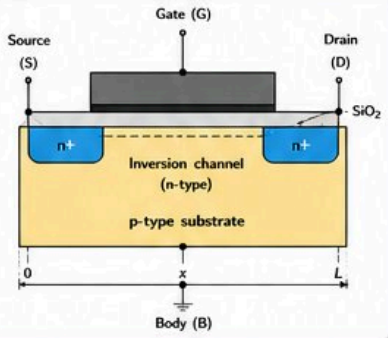


DRAIN CURRENT (I_D) AND ITS DERIVATION (n-CHANNEL MOSFET)

1. Introduction

- In an n-channel enhancement MOSFET, when $V_{GS} > V_{TH}$ and $V_{DS} > 0$, an inversion channel is formed and electrons flow from drain to source.
- The drain current I_D depends on V_{GS}, V_{DS} and device parameters.

2. Device Structure and Channell



3. Channel Charge and Inversion Layer

- The inversion charge per unit area (sheet charge) under the gate at a point x ($0 \le x \le L$) is

$$Q_{inv}(x) = -C_{ox}\,[V_{GS} - V_{TH} - V(x)]$$

where

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \text{(oxide capacitance per unit area)}$$

$V(x)$ = channel potential at position x.

- The channel charge is negative (electrons).

4. Channel Potential and Field

- Let $V(x)$ be the channel potential measured from source.
- At source ($x=0$): $V(0) = 0$
  At drain ($x=L$): $V(L) = V_{DS}$
- The lateral electric field in the channel is

$$E_x = -\frac{dV}{dx}$$

5. Derivation of Drain Current

Step 1: Current in a Small Slice

Consider a small slice of channel of length dx at position x.

The charge in this slice is

$$dQ = Q_{inv}(x)\; W\; dx$$

(W = channel width)

The drift current due to this charge is

$$dI_D = \mu_n \frac{dQ}{dx}\; E_x$$

where μ_n = electron mobility.

Step 2: Substitute Expressions

Substitute dQ and E_x,

$$dI_D = \mu_n \left[-C_{ox}\,(V_{GS} - V_{TH} - V(x))\; W\right] \left(-\frac{dV}{dx}\right)$$

$$dI_D = \mu_n C_{ox} W\,[V_{GS} - V_{TH} - V(x)]\,dV$$

Step 3: Integrate Along the Channel

Integrate from source (V=0) to drain (V=V_{DS}):

$$I_D = \int_0^{V_{DS}} \mu_n C_{ox} W\,[V_{GS} - V_{TH} - V]\,dV$$

$$= \mu_n C_{ox} W \left[(V_{GS} - V_{TH})V - \frac{V^2}{2}\right]_0^{V_{DS}}$$

$$I_D = \mu_n C_{ox} W \left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

(valid while the channel exists uniformly)

Step 4: Condition for Channel Existence

The channel exists as long as $V_{GS} - V_{TH} - V(x) > 0$.

At the drain end ($x = L$):

$$V_{GS} - V_{TH} - V_{DS} > 0$$

$$V_{DS} < V_{GS} - V_{TH}$$

This is the **linear (triode)** region.

6. Drain Current Expressions

(a) Linear / Triode Region ($0 < V_{DS} < V_{GS} - V_{TH}$)

From the above derivation,

$$I_D = \mu_n C_{ox} W \left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

or

$$I_D = k_n \left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

where $k_n = \mu_n C_{ox} W$

(b) Saturation Region ($V_{DS} \ge V_{GS} - V_{TH}$)

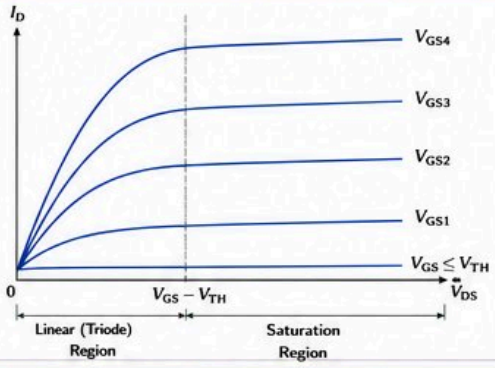
At $V_{DS} = V_{GS} - V_{TH}$, the channel is just pinched off at the drain. Current becomes independent of V_{DS} (ideally). Substituting $V_{DS} = V_{GS} - V_{TH}$ in the linear expression:

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox} W\,(V_{GS} - V_{TH})^2$$

or

$$I_{D,sat} = \frac{k_n}{2}\,(V_{GS} - V_{TH})^2$$

7. I_D–V_{DS} Characteristics (for Different V_{GS})



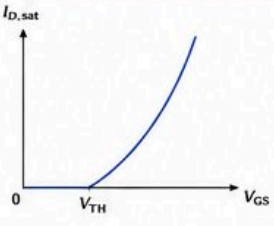
As V_{GS} increases, I_D increases.

In saturation, I_D is nearly constant (ideally).

8. I_D–V_{GS} Characteristics (Transfer Characteristic)

In saturation region,

$$I_{D,sat} = \frac{k_n}{2}\,(V_{GS} - V_{TH})^2 \quad \text{for } V_{GS} \ge V_{TH}$$

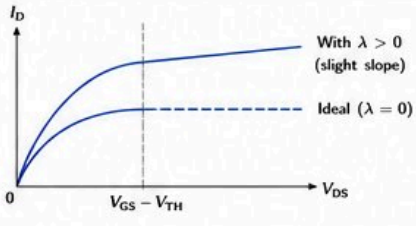


9. Effect of Channel Length Modulation (non-ideal)

In practice, I_D in saturation increases slightly with V_{DS} due to channel length modulation.

$$I_D = \frac{k_n}{2}\,(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (\text{for } V_{DS} \ge V_{GS} - V_{TH})$$

where λ = channel length modulation parameter (usually small).



10. Threshold Voltage (for reference)

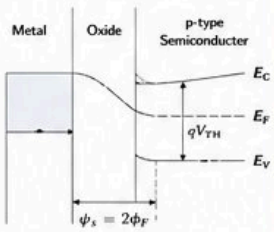
At threshold, $\psi_s = 2\phi_F$

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_s q N_A \phi_F}}{C_{ox}}$$

where

- V_{FB} = flat-band voltage
- ϕ_F = Fermi potential $= \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$
- N_A = substrate doping (acceptor)
- ε_s = semiconductor permittivity
- q = electron charge
- $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

Energy band diagram at threshold



11. Summary of Drain Current Equations

Region	Condition	Drain Current Expression
Linear (Triode)	$0 < V_{DS} < V_{GS} - V_{TH}$	$I_D = \mu_n C_{ox} W \left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] = k_n \left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$
Saturation (Ideal)	$V_{DS} \ge V_{GS} - V_{TH}$	$I_{D,sat} = \frac{1}{2}\mu_n C_{ox} W (V_{GS} - V_{TH})^2 = \frac{k_n}{2}(V_{GS} - V_{TH})^2$
Saturation (Non-ideal)	$V_{DS} \ge V_{GS} - V_{TH}$	$I_D = \frac{k_n}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$

Where

- $k_n = \mu_n C_{ox} W$
- $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$
- W = Channel width
- L = Channel length
- μ_n = Electron mobility
- V_{TH} = Threshold voltage

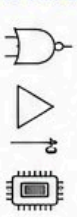
12. Key Points

- ✓ Drain current flows when $V_{GS} > V_{TH}$.
- ✓ In linear region, I_D increases linearly with V_{DS} at small V_{DS}, then curves.
- ✓ In saturation region, I_D is almost constant (ideally) and depends on $(V_{GS} - V_{TH})^2$.
- ✓ Threshold voltage depends on work function difference, oxide thickness and substrate doping.
- ✓ Long channel assumption used in derivation.

13. Assumptions in Derivation

- Gradual channel approximation (electric field primarily along channel).
- Constant mobility (μ_n).
- No velocity saturation.
- No channel length modulation (for ideal case).
- Uniform doping in substrate.

14. Applications



- Digital ICs (CMOS logic gates, memories)
- Analog amplifiers and buffers
- Switching applications (power MOSFETs)
- RF circuits and mixed-signal ICs

15. Note

The above equations are for n-channel enhancement MOSFET.

For p-channel devices, current direction and polarities are reversed.

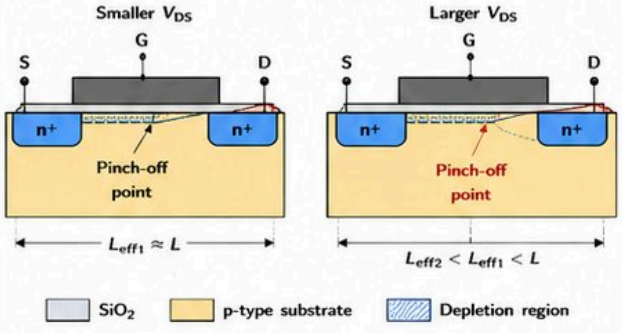
CHANNEL LENGTH MODULATION (λ) IN MOSFET

1. Introduction

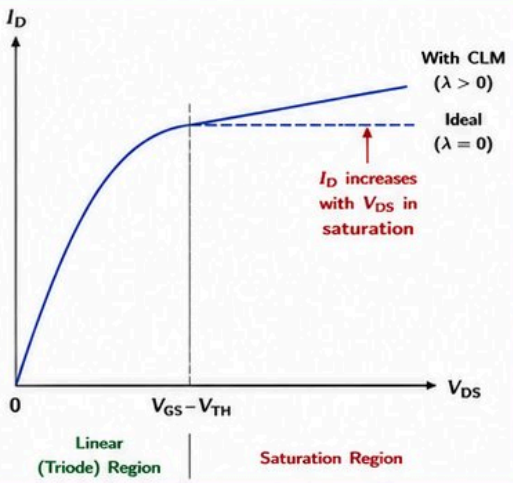
- In an ideal MOSFET, when the device operates in saturation ($V_{DS} \geq V_{GS} - V_{TH}$), I_D is independent of V_{DS}.
- In practice, I_D increases slightly with V_{DS} due to the shortening of the effective channel length.
- This effect is called **Channel Length Modulation** (CLM).
- It is modeled by parameter λ (channel length modulation parameter).

2. Physical Explanation

In saturation, the channel is pinched off near the drain. As V_{DS} increases, the depletion region widens more into the channel, reducing the effective channel length (L_{eff}). The shorter channel offers less resistance, so I_D increases slightly.



3. Effect on I_D–V_{DS} Characteristics



4. Derivation of CLM Effect

In saturation, the saturation current without CLM is

$$I_{D,sat(ideal)} = \frac{k_n}{2}(V_{GS} - V_{TH})^2$$

Due to CLM, the effective channel length becomes $L_{eff} < L$.

Since $I_D \propto \frac{1}{L_{eff}}$, we can write

$$I_{D,sat} \propto \frac{1}{L_{eff}} \propto \frac{1}{L - \Delta L}$$

When V_{DS} increases, the depletion region extends by ΔL into the channel. For small $\Delta L \ll L$,

$$\frac{1}{L - \Delta L} = \frac{1}{L}\frac{1}{1 - \Delta L/L} \approx \frac{1}{L}\left(1 + \frac{\Delta L}{L}\right)$$

Since $\frac{\Delta L}{L}$ is approximately proportional to V_{DS},

$$I_{D,sat} \approx \frac{k_n}{2}(V_{GS} - V_{TH})^2\left(1 + \lambda V_{DS}\right)$$

where $\lambda = \frac{1}{L}\frac{d(\Delta L)}{dV_{DS}}$ (approximately constant).

5. Saturation Current with CLM

$$I_D = \frac{k_n}{2}(V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

for $V_{DS} \geq V_{GS} - V_{TH}$

where

$k_n = \mu_n C_{ox} \frac{W}{L}$ (process transconductance parameter)

λ = channel length modulation parameter (V^{-1})

λ is typically in the range of 0.01 to 0.2 V^{-1}.

Interpretation:

- When $\lambda = 0$ (ideal case):
  I_D is independent of V_{DS} in saturation.
- When $\lambda > 0$ (practical case):
  I_D increases linearly with V_{DS} in saturation.

6. Output Resistance due to CLM

In saturation region,

$$I_D = I_{D0}(1 + \lambda V_{DS})$$

where $I_{D0} = \frac{k_n}{2}(V_{GS} - V_{TH})^2$

The small-signal output conductance g_{ds} is

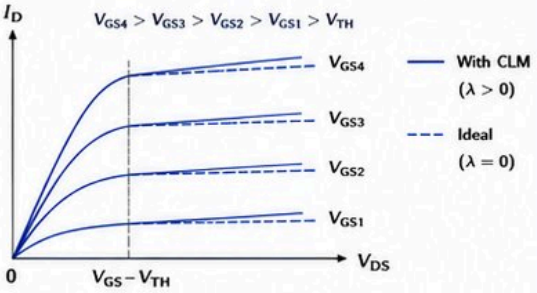
$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}}\bigg|_{V_{GS}} = I_{D0}\lambda = \lambda I_D$$

Thus, the output resistance r_o is

$$r_o = \frac{1}{g_{ds}} = \frac{1}{\lambda I_D}$$

Key Point:
CLM introduces a finite output resistance r_o, which is inversely proportional to λ and I_D.

7. Effect of λ on Output Characteristics



Larger λ → Larger slope in saturation
Smaller λ → Flatter curves (closer to ideal)

8. Typical Values of λ

Technology	λ (V^{-1}) Typical Range
Old (Micron & above)	0.1 – 0.2
0.5 µm	0.05 – 0.1
0.18 µm	0.02 – 0.05
90 nm	0.01 – 0.03
45 nm and below	0.005 – 0.02

As technology scales down, λ generally decreases (slightly) due to improved channel control.

9. Summary

- ☑ Channel length modulation is caused by the reduction of effective channel length in saturation.
- ☑ It makes I_D increase linearly with V_{DS} in saturation.
- ☑ Modeled by: $I_D = \frac{k_n}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$ for $V_{DS} \geq V_{GS} - V_{TH}$
- ☑ CLM introduces finite output resistance: $r_o = \frac{1}{\lambda I_D}$
- ☑ Smaller λ → Higher r_o → Better current source.

Important Notes

- CLM does not affect the triode (linear) region equation.
- CLM is an important second-order effect in analog/Mixed-Signal design (e.g., current mirrors, amplifiers).

Practical Impact

- ★ Increases output conductance (g_{ds}), decreases output resistance (r_o).
- ★ Affects gain, current mirror accuracy, and biasing in analog circuits.

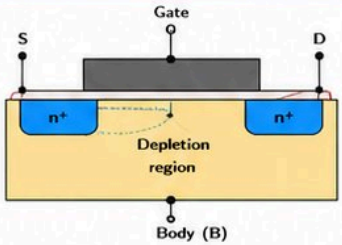
BODY BIAS EFFECT (SUBSTRATE BIAS EFFECT) IN MOSFET

Effect of Source–Body Voltage (V_{SB}) on Threshold Voltage and Drain Current

1. Introduction

- In a MOSFET, the threshold voltage depends on the source–body voltage (V_{SB}).
- When the body is not at the same potential as the source, the depletion region charge changes.
- This effect is called **Body Bias Effect** or **Substrate Bias Effect**.
- It is widely used in circuit design (e.g., body biasing for performance/power optimization).

2. Physical Explanation



If the body is made more negative with respect to the source ($V_{SB} > 0$ for NMOS), the depletion region widens.
More charge is required to invert the surface, so the threshold voltage increases.

n+ p-type body Depletion region

3. Threshold Voltage with Body Bias

The threshold voltage with body bias is given by the well-known body effect equation:

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$

where

- V_{TH0} = Threshold voltage at $V_{SB} = 0$
- V_{SB} = Source–Body voltage (for NMOS, $V_{SB} \geq 0$)
- ϕ_F = Fermi potential $= \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right)$
- γ = Body effect coefficient ($V^{1/2}$)

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

N_A = Body doping, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

4. Body Effect Coefficient (γ)

It indicates how sensitive the threshold voltage is to body bias.

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

where

ε_{si} = Permittivity of silicon
N_A = Body (substrate) doping
C_{ox} = Oxide capacitance per unit area

Observation:

- Higher body doping (N_A) → Higher γ
- Thicker oxide (t_{ox}) → Lower γ

5. Effect on Threshold Voltage (NMOS)

For NMOS:

- If $V_{SB} > 0$ (body more negative than source): V_{TH} increases
- If $V_{SB} = 0$: $V_{TH} = V_{TH0}$ (no body effect)
- If $V_{SB} < 0$ (body more positive than source): V_{TH} decreases (not commonly used for NMOS)

For PMOS, the polarities are reversed.

6. Effect on Drain Current

Since I_D depends on V_{TH}, the body bias also affects I_D.

In saturation region (with CLM):

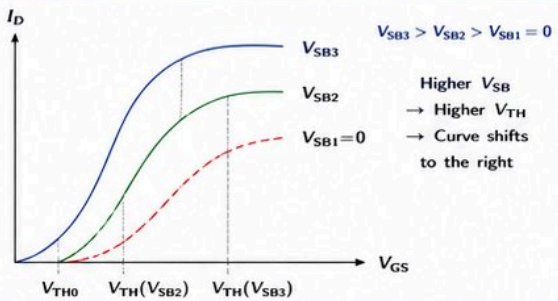
$$I_D = \frac{k_n}{2} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

With body bias,

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$

Thus, higher V_{SB} → higher V_{TH} → lower I_D (lower current for the same V_{GS}).

7. I_D–V_{GS} Characteristics for Different V_{SB}



8. Derivation of Body Effect Equation

From the derivation of threshold voltage,

$$V_{TH} = V_{FB} + 2\phi_F + \frac{|Q_{dep,max}|}{C_{ox}}$$

At threshold, the maximum depletion charge is

$$Q_{dep,max} = -\sqrt{2q\varepsilon_{si}N_A(2\phi_F + V_{SB})}$$

Substituting,

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\varepsilon_{si}N_A(2\phi_F + V_{SB})}}{C_{ox}}$$

Let $V_{TH0} = V_{FB} + 2\phi_F + \frac{\sqrt{4q\varepsilon_{si}N_A\phi_F}}{C_{ox}}$
(represent value at $V_{SB} = 0$)

After simplification,

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$

where $\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$

9. Typical Values (NMOS)

Parameter	Typical Value
V_{TH0}	0.35 – 0.50 V
ϕ_F	0.25 – 0.35 V
γ	0.3 – 0.7 $V^{1/2}$
V_{SB} (usable range)	0 to 0.8 V
Effect on V_{TH}	50 – 150 mV increase (typical)

Example:

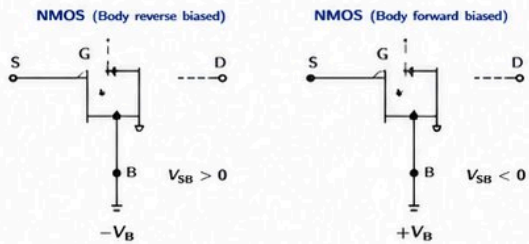
Given: $V_{TH0} = 0.40$ V, $\gamma = 0.4$ $V^{1/2}$, $\phi_F = 0.3$ V

For $V_{SB} = 0.4$ V,

$$V_{TH} = 0.40 + 0.4 \left(\sqrt{2(0.3) + 0.4} - \sqrt{2(0.3)} \right)$$
$$= 0.40 + 0.4(1.095 - 0.775) = 0.40 + 0.128$$
$$= 0.528 \text{ V}$$

10. Practical Applications

- Used in body biasing techniques to control V_{TH} dynamically.
- Forward body bias ($V_{SB} < 0$ for NMOS) → lowers V_{TH} → faster circuits.
- Reverse body bias ($V_{SB} > 0$ for NMOS) → raises V_{TH} → reduces leakage → saves power.
- Widely used in adaptive body bias (ABB), DTMOS, and low-power designs.



11. Key Points

- ✓ Threshold voltage increases with V_{SB} for NMOS.
- ✓ Given by: $V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$
- ✓ Higher V_{SB} → wider depletion region → higher V_{TH} → lower I_D.
- ✓ Body effect coefficient γ depends on doping and oxide thickness.

12. Summary

Body bias (substrate bias) changes the electric field in the body region, which alters the depletion charge and hence the threshold voltage.

It is a powerful technique for performance tuning and leakage control in modern CMOS technologies.

13. Note

This effect is significant in short-channel devices where body biasing is commonly used for adaptive performance and power optimization.

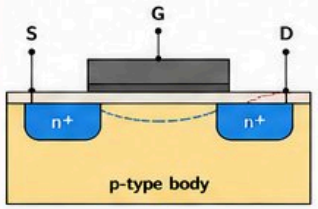
SHORT CHANNEL EFFECTS (SCE) IN MOSFET

1. Introduction

- As the channel length (L) becomes comparable to the depletion width and oxide thickness, the electric field from the drain strongly influences the channel.
- This leads to deviation from ideal long channel behavior.
- These phenomena are called **Short Channel Effects (SCE)**.
- SCE causes: higher off-state current, lower threshold voltage, mobility reduction, and reduced output resistance.

2. Ideal Long-Channel vs Short-Channel

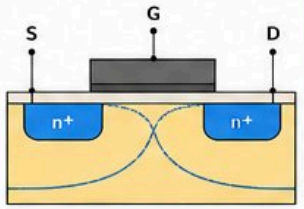
Long Channel (Ideal)



Depletion region mainly from source. Drain has little control.

$L \gg$ depletion width

Short Channel ($L \downarrow$)



Depletion regions from source and drain overlap and are controlled by both S and D.

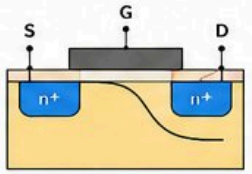
$L \approx$ depletion width

3. Major Short Channel Effects

1. **Threshold Voltage Roll-off ($V_{TH} \downarrow$)**
   V_{TH} decreases as channel length decreases.
2. **Drain Induced Barrier Lowering (DIBL)**
   Drain voltage lowers the source-channel barrier, reducing V_{TH}.
3. **Subthreshold Swing Degradation (SS $\uparrow$)**
   Weaker gate control → less steep subthreshold slope.
4. **Increase in Off-State Current ($I_{OFF} \uparrow$)**
   Lower V_{TH} and DIBL → more leakage.
5. **Mobility Degradation ($\mu_{eff} \downarrow$)**
   Surface scattering $\uparrow$ due to high vertical field.
6. **Velocity Saturation (v_{sat})**
   High lateral field near drain → carrier velocity saturates.

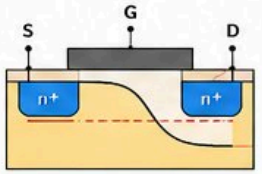
4. Drain Induced Barrier Lowering (DIBL)

Low V_{DS}



High barrier → high V_{TH}

High V_{DS}

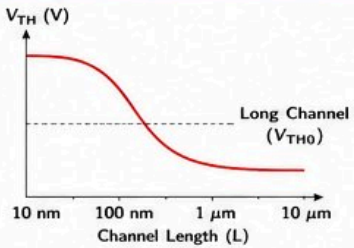


Barrier lowered by drain field → lower V_{TH}

$$\text{DIBL} = \frac{V_{TH}(V_{DS}=\text{low}) - V_{TH}(V_{DS}=\text{high})}{V_{DS}(\text{high}) - V_{DS}(\text{low})}$$

Higher DIBL → stronger short channel effect

5. Threshold Voltage Roll-Off



As L decreases, V_{TH} decreases below the long channel value (V_{TH0}).
Reason: charge sharing between source and drain depleted regions.

Empirical Model

$$V_{TH}(L) = V_{TH0} - \frac{\Delta V_{TH}}{1 + L/L_{ref}}$$

where

V_{TH0} = long channel threshold voltage

ΔV_{TH} = roll-off magnitude

L_{ref} = characteristic length

6. Subthreshold Swinge Degradation

Subthreshold swing (SS):

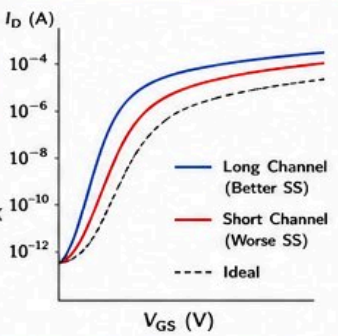
$$SS = \frac{dV_{GS}}{d(\log_{10} I_D)} \quad \text{(V/decade)}$$

Ideal MOSFET:

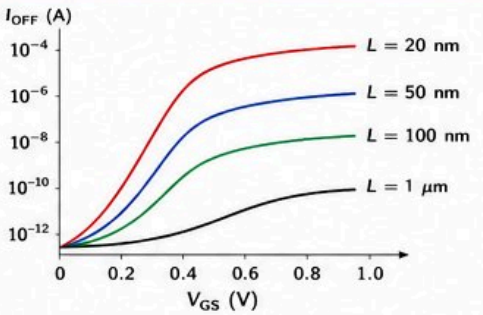
$$SS_{ideal} = 2.303 \frac{kT}{q} \approx 60 \text{ mV/dec at } 300\text{K}$$

Short channel:

SS increases due to weak gate control.



7. Off-State Current Increase



Shorter channel length → higher I_{OFF} due to:

- Lower V_{TH}
- DIBL
- Punch-through

8. Mobility Degradation

Strong vertical electric field near the surface causes:

- Increased surface scattering
- Reduced effective mobility (μ_{eff})

$\mu_{eff} < \mu_0$

μ_{eff} decreases as:

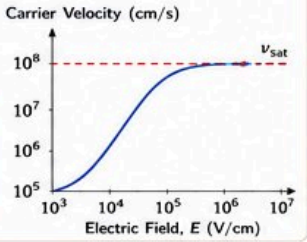
- L decreases
- V_{GS} increases
- E_{ox} (gate oxide field) increases

9. Velocity Saturation

At high lateral field (near drain), carrier velocity does not increase indefinitely, but saturates at v_{sat}.

$$v = \frac{\mu E}{1 + \mu E / v_{sat}} \xrightarrow{E \to \infty} v_{sat}$$

$v_{sat} \approx (1-2) \times 10^7$ cm/s



10. Summary of SCE Impacts

Parameter	Effect of Shorter L	Reason
V_{TH}	Decreases ↓	Threshold roll-off, DIBL
I_{OFF}	Increases ↑	Lower V_{TH}, leakage
SS	Increases (worse) ↑	Weak gate control
μ_{eff}	Decreases ↓	Surface scattering
I_D (sat)	Decreases slightly ↓	Mobility degradation
Output Resistance (r_o)	Decreases ↓	Channel length modulation, DIBL

11. Scaling Guidelines

To reduce SCE:

- Use thinner gate oxide ($t_{ox} \downarrow$)
- Lower body doping ($N_A \downarrow$)
- Use high-κ dielectrics
- Use multi-gate structures (FinFET, GAA, SOI)
- Optimize halo/ pocket implants
- Use raised source/drain

12. Key Points

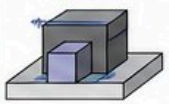
- ✓ SCE become significant when L is comparable to depletion width and t_{ox}.
- ✓ DIBL, V_{TH} roll-off and mobility degradation are main issues.
- ✓ These effects limit scaling and increase power consumption.
- ✓ Advanced device structures are used to control SCE.

13. Typical Technology Trend

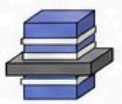
Technology Node	180 nm	90 nm	45 nm	22 nm	7 nm
Channel Length (nm)	~180	~90	~45	~22	~7
DIBL (mV/V)	~50	~100	~150	~200	> 250
V_{TH} Roll-off (mV)	~40	~80	~120	~160	> 200
I_{OFF} Increase	Slight	Moderate	High	Very High	Extreme

14. Modern Solutions

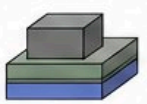
FinFET (3-Gate)



Gate-All-Around (GAA)



FD-SOI



- Better electrostatic control
- Reduced SCE
- Lower leakage
- Higher drive current

MOSFET AS A SWITCH (MOS AS A SWITCH)

A MOSFET operates in two extreme regions as a switch: OFF (Cut-Off) and ON (Triode/Linear)

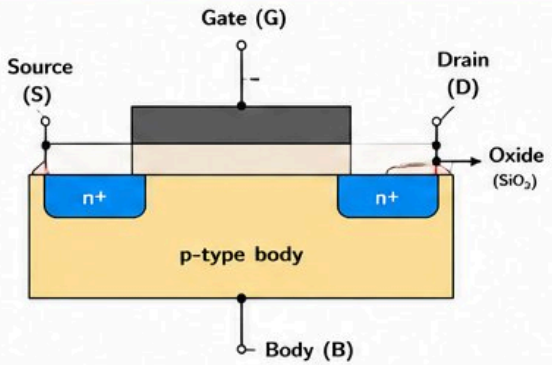
1. Introduction

- A MOSFET can be used as an electronic switch.
- It has three terminals: Gate (G), Drain (D), Source (S) and Body (B).
- A small voltage at the gate controls a large current between drain and source.

Two states:

- OFF State → Open Switch
- ON State → Closed Switch

2. MOSFET Structure (n-Channel Enhancement)



3. Switch States at a Glance

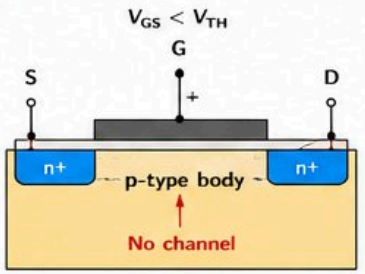
State	Gate Condition (V_{GS})	Drain–Source Behavior	Equivalent Circuit	Symbol
OFF (Cut-Off)	$V_{GS} < V_{TH}$	No channel formed. $I_D \approx 0$ (Only leakage) Open circuit between D and S.	Open Switch D S	D G S
ON (Triode/Linear)	$V_{GS} > V_{TH}$ and V_{DS} is small (≈ 0)	Strong channel formed. Low resistance path between D and S. I_D is large.	Closed Switch D S	D G S

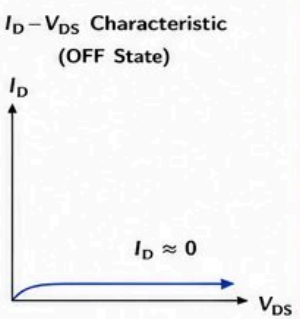
4. OFF State (Cut-Off)

Condition:

$V_{GS} < V_{TH}$

- No inversion channel is formed.
- Drain and source are isolated.
- $I_D \approx 0$ (only leakage)
- MOSFET behaves as an OPEN SWITCH.





5. ON State (Triode/Linear)

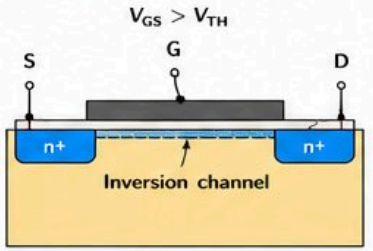
Conditions:

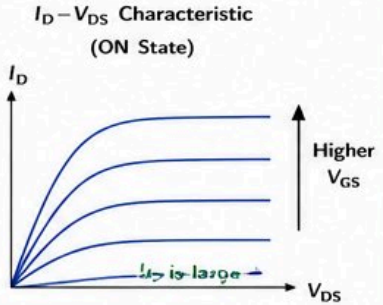
$V_{GS} > V_{TH}$

and

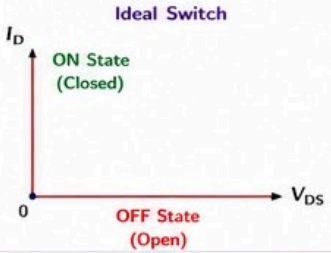
$V_{DS} \approx 0$ (small)

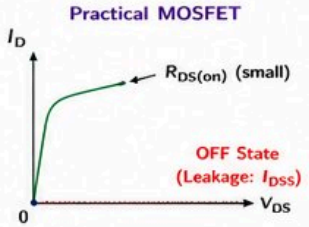
- Inversion channel is formed.
- Low on-resistance.
- I_D is large.
- MOSFET behaves as a CLOSED SWITCH.





6. I–V View of Switch Operation





Key Parameter (ON State)

$$R_{DS(on)} = \left.\frac{V_{DS}}{I_D}\right|_{V_{GS}\text{ fixed}}$$

Lower $R_{DS(on)}$ → Better switch (higher current, lower loss)

7. Truth Table (n-Channel Enhancement)

V_{GS}	Switch State	Equivalent Circuit
$V_{GS} < V_{TH}$	OFF (Open)	D S
$V_{GS} > V_{TH}$	ON (Closed)	D S

8. Application Examples

- Digital ICs (CMOS logic switches)
- Power management (DC–DC converters)
- Load switching
- Motor drivers, relays, solid-state switches

9. Summary

- When $V_{GS} < V_{TH}$ → no channel → $I_D \approx 0$ → OPEN SWITCH.
- When $V_{GS} > V_{TH}$ and $V_{GS} \approx 0$ → channel formed → low $R_{DS(on)}$ → CLOSED SWITCH.
- A MOSFET is a voltage-controlled switch with high input impedance and fast operation.

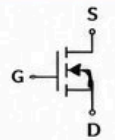
10. Important Notes

- For p-channel MOSFET, polarities are reversed. (Use negative V_{GS} to turn ON.)
- Never use in the linear region (moderate V_{DS}) for switching – it increases power dissipation.
- Always operate either in Cut-Off (OFF) or Triode (ON with small V_{DS}).

p-Channel Switch (Summary)

ON → $V_{GS} < -|V_{TH}|$

OFF → $V_{GS} > -|V_{TH}|$

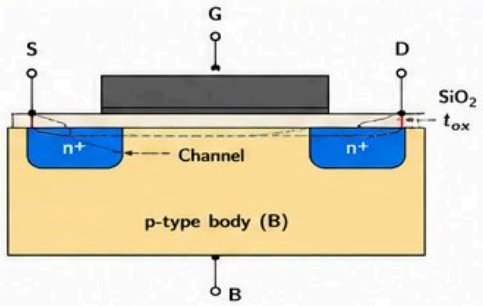


MOSFET CAPACITANCE (n-CHANNEL ENHANCEMENT MOSFET)

1. Introduction

- MOSFET has capacitances between its terminals due to overlap of depletion regions, gate oxide and inversion channel.
- These capacitances affect switching speed, delay, power and RF performance.
- Capacitances are voltage dependent.
- There are two types:
  1. Intrinsic (Internal) Capacitances
  2. Extrinsic (Parasitic) Capacitances

2. Device Structure (n-MOSFET)



3. Types of Capacitances

(A) Intrinsic (Internal) Capacitances

- Between gate and channel regions.
- Mainly due to gate oxide.

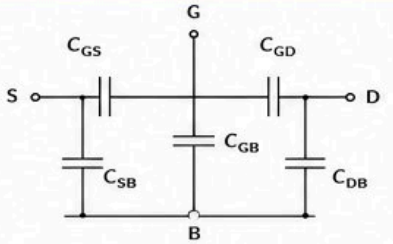
C_{GS} , C_{GD} , C_{GB}

(B) Extrinsic (Parasitic) Capacitances

- Due to overlap of depletion regions with gate and source/drain.
- Voltage independent (approx.).

C_{ovGS} , C_{ovGD}

4. Capacitance Model



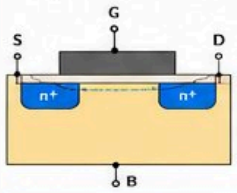
Intrinsic: C_{GS}, C_{GD}, C_{GB}

Extrinsic: C_{ovGS}, C_{ovGD} (included in C_{GS}, C_{GD})

5. Intrinsic Capacitances – Physical Origin

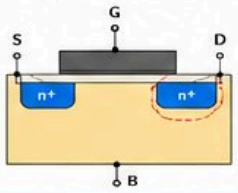
(i) C_{GS} (Gate–Source)

Gate overlap source depletion region and channel.



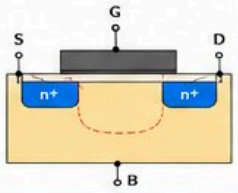
(ii) C_{GD} (Gate–Drain)

Gate overlap drain depletion region and channel.



(iii) C_{GB} (Gate–Body)

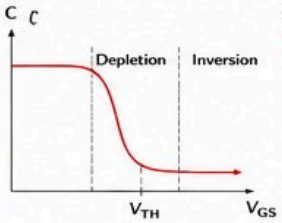
Gate overlap body depletion region.



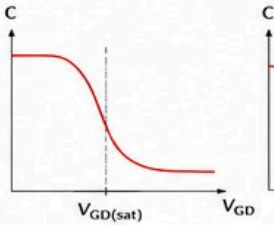
These capacitances depend on the bias voltages (V_{GS}, V_{GD}, V_{SB}) and region of operation.

6. Capacitance–Voltage Characteristics (Typical)

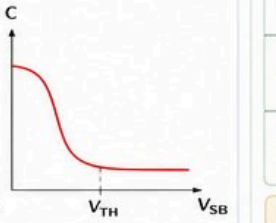
C_{GS} vs V_{GS} (V_{DS} constant)



C_{GD} vs V_{GD} (V_{GS} constant)



C_{GB} vs V_{SB} (V_{GS}, V_{DS} constant)



- Capacitances decrease as reverse bias across depletion region increases.

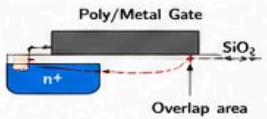
7. Intrinsic Capacitance Expressions (Approx.)

C_{GS}	$C_{GS} = C_{ox}\frac{W}{L}(x_d + x_i)$	x_d : depletion width on source side x_i : channel length in inversion
C_{GD}	$C_{GD} = C_{ox}\frac{W}{L}x_d$	x_d : depletion width on drain side
C_{GB}	$C_{GB} = C_{ox}\frac{W}{L}x_b$	x_b : depletion width into body

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$: oxide capacitance per unit area

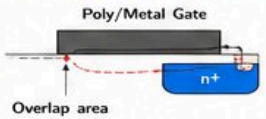
8. Extrinsic (Parasitic) Capacitances

(i) Gate–Source Overlap (C_{ovGS})



$C_{ovGS} = C_{ox}\frac{W}{L_{ov}}$

(ii) Gate–Drain Overlap (C_{ovGD})



$C_{ovGD} = C_{ox}\frac{W}{L_{ov}}$

L_{ov} = overlap length (technology dependent)
These are nearly voltage independent.

9. Total Gate Capacitances (including Overlap)

$C_{GS(total)} = C_{GS} + C_{ovGS}$

$C_{GD(total)} = C_{GD} + C_{ovGD}$

$C_{GB(total)} = C_{GB}$ (No overlap term normally)

In small geometry (short channel), overlap and fringing capacitances become significant.

10. Capacitance in Different Regions (Qualitative)

Region	C_{GS}	C_{GD}	C_{GB}
Cut-off ($V_{GS} < V_{TH}$)	Small ($\sim C_{ovGS}$)	Small ($\sim C_{ovGD}$)	$C_{ox}\frac{W}{L}x_b$ (Moderate)
Linear ($0 < V_{DS} < V_{GS} - V_{TH}$)	Moderate	Moderate	Moderate
Saturation ($V_{DS} \geq V_{GS} - V_{TH}$)	High ($\approx C_{ox}\frac{W}{L}$)	Small	Moderate

11. Effects of Capacitances

- Gate capacitances (C_{GS}, C_{GD}) charge/discharge during switching → affect speed and delay.
- Miller effect: C_{GD} appears multiplied by $(1 - A_v)$ during amplification.
- Higher capacitance → slower operation, higher dynamic power ($P = CV^2f$).
- Important in analog/RF (gain, bandwidth).

12. Key Points

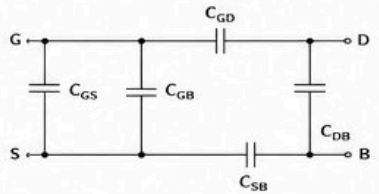
- ✓ MOSFET has intrinsic (C_{GS}, C_{GD}, C_{GB}) and extrinsic (C_{ovGS}, C_{ovGD}) capacitances.
- ✓ Intrinsic capacitances are voltage and region dependent.
- ✓ Extrinsic (overlap) capacitances are nearly constant.
- ✓ Total gate capacitances = intrinsic + overlap.
- ✓ Smaller dimensions → smaller capacitance but overlap becomes more important.

13. Typical Values (Example: 65 nm nMOS)

Parameter	Typical Range (per μm width)
C_{ox}	~ 1.5 – 2.5 fF/μm²
C_{ovGS}, C_{ovGD}	~ 0.1 – 0.3 fF/μm
C_{GS} (inversion)	~ 1 – 2 fF/μm
C_{GD} (saturation)	~ 0.1 – 0.3 fF/μm
C_{GB}	~ 0.1 – 0.5 fF/μm

(Values vary with technology and bias)

14. Frequency Equivalent Model (Small Signal)



At high frequency, these capacitances provide AC paths and affect gain, bandwidth and stability.

15. Applications

- Digital integrated circuits (switching, timing).
- Analog/RF amplifiers (gain, bandwidth).
- High-speed design and low-power optimization.
- Device modeling (SPICE: BSIM, EKV).

Capacitances may be obtained from device models, datasheets or extracted using TCAD / SPICE simulations.

MOSFET MODELS FOR CALCULATION AND TRANSISTOR LAYOUT

A. MOSFET Models for Calculation

1. Purpose of Models

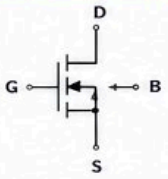
- MOSFET models describe the I–V behavior using simple equivalent circuits and equations.
- Models range from simple (hand) models to accurate SPICE models.

2. Levels of MOSFET Models

Model Level	Name / Example	Use	Accuracy	Complexity
Level 1	Square-Law Model	Hand calculation, concept	Low	Very Low
Level 2	Shichman–Hodges (Model Level 1/ 2)	Circuit analysis, analog design	Medium	Low
Level 3	BSIM3	General purpose IC design	High	Medium
Level 4	BSIM4 / BSIM-CMG	Deep submicron technologies	Very High	High

3. Common Hand Calculation Model (Square-Law Model)

Circuit Symbol (nMOS)



Regions of Operation

1. Cut-off: $V_{GS} \le V_{TH}$, $I_D \approx 0$
2. Triode (Linear): $V_{GS} > V_{TH}$, $V_{DS} < V_{GS} - V_{TH}$
3. Saturation: $V_{GS} > V_{TH}$, $V_{DS} \ge V_{GS} - V_{TH}$

I_D Equations (Long Channel)

1. Triode (Linear) Region

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

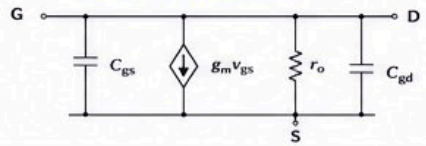
2. Saturation Region

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

where $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, λ = channel length modulation

4. Small-Signal Model (Saturation Region)

Small-signal equivalent circuit



$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) \quad \text{(saturation)}$$

$$r_o = \frac{1}{\lambda I_D} \quad \text{(due to channel length modulation)}$$

5. Shichman–Hodges (Level 1/2) Model

- Includes long channel effects with body effect and channel length modulation.
- Threshold voltage with body effect:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

- Drain current equations same as square-law with V_{TH} above (include λ for saturation).

6. BSIM Model (BSIM3/4)

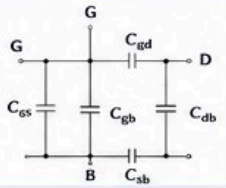
- Physically based: includes short channel effects, mobility degradation, velocity saturation, DIBL, etc.
- Used in SPICE simulators.

Geometry (W, L, t_{ox}, N_A, ...) → BSIM Equations (Physical Model) → I–V Characteristics (I_D, g_m, C_{ij}, ...)

7. Capacitance Model (Used in AC/Transient Analysis)

Intrinsic Capacitances

- C_{gs} : gate-source capacitance
- C_{gd} : gate-drain capacitance
- C_{gb} : gate-body capacitance
- C_{db} : drain-body capacitance
- C_{sb} : source-body capacitance



8. Summary

- Use square-law model for quick hand calculations and understanding.
- Use Level 1/2 (Shichman–Hodges) for basic analog design.
- Use BSIM models in SPICE for accurate simulation of modern technologies.

Typical Parameters

μ_n: electron mobility

$C_{ox} = \varepsilon_{ox} / t_{ox}$

W, L : width and length

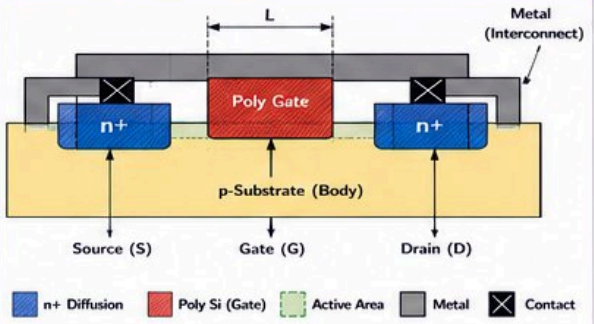
V_{TH0}: threshold voltage (zero body bias)

γ : body effect coefficient

λ : channel length modulation

B. Transistor Layout (nMOS Example)

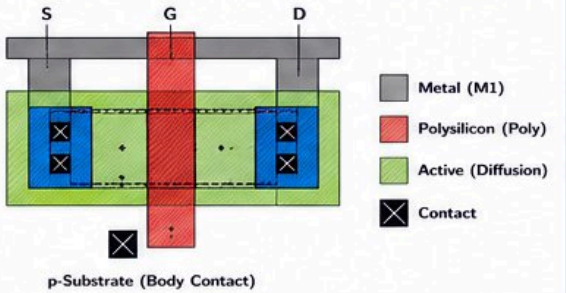
1. Basic Layout Structure



2. Layout Layers (Typical CMOS Process)

Layer	Purpose / Description
N-Well	Well region for PMOS
Active (Diffusion)	Defines source/drain regions
Polysilicon (Poly)	Forms the gate
Gate Oxide	Thin oxide under the gate
Contact	Connects diffusion/poly to metal
Metal (M1, M2, ...)	Interconnects between devices
Via	Connects between metal layers
Passivation	Protects the device

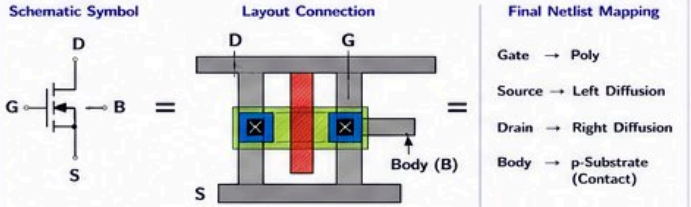
3. Top View Layout (nMOS)



4. Layout Design Rules (Typical)

Parameter	Description
L (Gate Length)	Minimum allowed gate length
W (Gate Width)	Transistor width (controls I_D)
t_{ox}	Gate oxide thickness
Spacing	Min spacing between layers
Overlap	Poly over diffusion (both sides)
Contact size	Min contact dimension
Metal width	Min metal line width

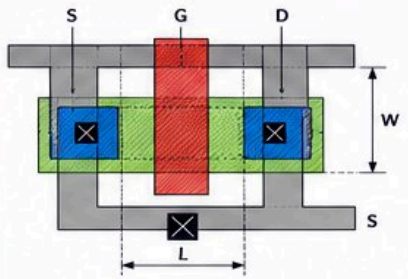
5. Layout Connection (Schematic vs Layout)



6. Good Layout Practices

- ✓ Keep L as minimum as per design.
- ✓ Increase W to get required I_D.
- ✓ Ensure proper contacts to reduce series resistance.
- ✓ Follow design rules (spacing, overlap, density).
- ✓ Use substrate contact to avoid floating body effect.

7. Example: nMOS Layout with Dimensions



Example Dimensions

Parameter	Value (Example)
L (Gate Length)	0.18 μm
W (Gate Width)	1.0 μm
t_{ox}	4 nm
Overlap (Poly-Active)	0.05 μm
Active Spacing	0.15 μm
Contact Size	0.15 × 0.15 μm
Metal Width	0.2 μm

8. Summary

- Layout converts schematic into physical structure.
- Proper layout ensures performance, yield and reliability.
- W controls current, L controls speed and power.
- Follow design rules strictly in modern technologies.

CMOS LAYOUT ELEMENTS

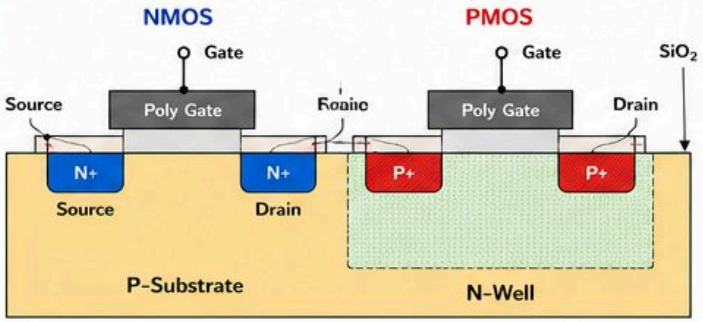
Building Blocks of CMOS VLSI Layout

1. Introduction

A CMOS layout is a geometric representation of transistors and interconnections on silicon.

It is composed of basic layers (elements) that form the devices and connect them to implement circuits.

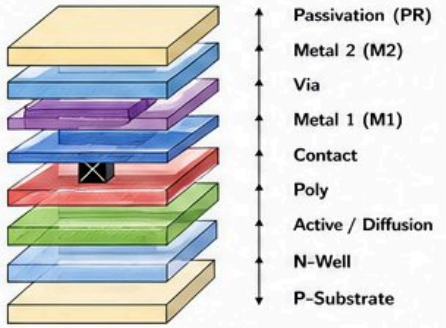
2. CMOS Fabrication Overview (Simplified Cross-Section)



3. Layout Layers (Typical N-Well CMOS Process)

Layer (Name)	Purpose	Typical Color
N-Well	Defines PMOS region	
Active / Diffusion	Transistor S/D regions	
Poly (Polysilicon)	Forms the gate	
Contact	Connects poly/diffusion to metal	
Metal 1 (M1)	First metal interconnect	
Via	Connects M1 to M2	
Metal 2 (M2)	Higher level interconnect	
Passivation (PR)	Protects the circuit	

4. Layout Layer Stack (From Bottom to Top)

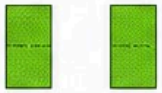


5. Basic Layout Elements

(a) N-Well

Region for PMOS transistors. Surrounded by P-substrate.

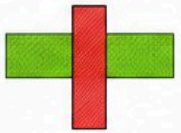
(b) Active / Diffusion



N+ Diffusion (NMOS S/D) P+ Diffusion (PMOS S/D)

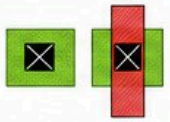
Where source/drain regions are formed.

(c) Poly (Polysilicon)



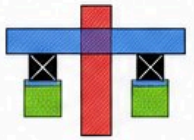
Forms the gate over active region.

(d) Contact



Creates electrical connection between poly/diffusion and metal.

(e) Metal (M1)



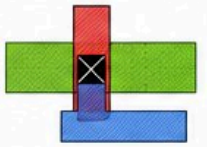
Used for interconnects (wires). Different layers can cross using vias.

(f) Via

Connects lower metal (M1) to upper metal (M2).

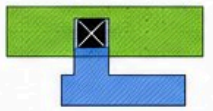
6. Common Composite Structures

(a) Poly Contact



Connects gate to metal (e.g., for gate input).

(b) Diffusion Contact



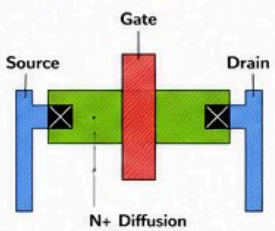
Connects source/drain to metal.

(c) Metal Crossing

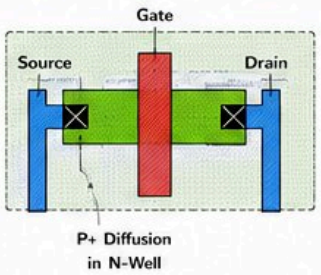
Two metal layers cross using via.

7. Transistor Layout Examples

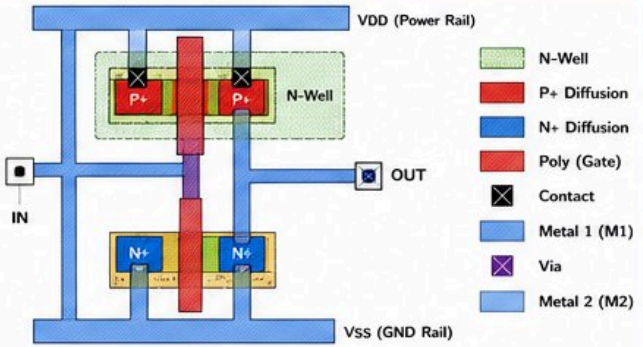
(a) NMOS Layout



(b) PMOS Layout (in N-Well)



8. Simple CMOS Inverter Layout



9. Design Rule Parameters (Typical)

Parameter	Description
L (Gate Length)	Minimum channel length
W (Transistor Width)	Minimum width
t_{ox}	Gate oxide thickness
Spacing	Min. spacing between layers
Overlap	Min. overlap (poly over active)
Contact Size	Min. contact dimensions
Metal Width	Min. metal line width
Via Size	Min. via dimensions

10. Key Points

- ✓ Layout is drawn layer by layer according to process rules.
- ✓ N-Well is needed only for PMOS devices.
- ✓ Contacts connect diffusion/poly to metal.
- ✓ Vias connect metal layers.
- ✓ Follow design rules for spacing, overlap, and widths.
- ✓ Good layout ensures working and manufacturable chips.

11. Common Layout Symbols and Colors (Reference)

N-Well | Active / Diffusion (N+, P+) | Poly (Polysilicon) | Contact | Metal 1 (M1) | Via | Metal 2 (M2) | Passivation (PR)

12. Typical Layout Flow

Schematic Capture → Layout Creation → Design Rule Check (DRC) → Layout vs Schematic (LVS) → Extraction (Parasitics) → Tape-out (GDSII)

PARASITIC, WIRE AND VIAS DESIGN RULES AND LAYOUT

1. Introduction

- Interconnect (wires and vias) create parasitic R, C, and L that affect speed, power and reliability.
- Design Rules (DRC rules) ensure manufacturability, yield and reliability.
- Layout must follow minimum dimensions for wires, spacing, overlaps, and via rules.

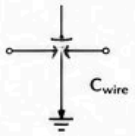
2. Parasitic Effects in Interconnects

Wire (Resistance)

$$R = \rho \frac{L}{W \cdot T}$$

ρ : resistivity, L: length, W: width, T: thickness

Wire (Capacitance)



$$C \approx C_{ox}\ P\ L$$

P: perimeter = $2(W+T)$

Wire (Inductance)

$$L \approx \mu_0 \mu_r \frac{L}{2\pi} \ln\left(\frac{2L}{W+T}\right)$$

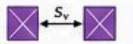
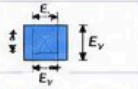
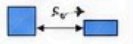
μ_0: vacuum permeability, μ_r: relative permeability

Longer wire → Higher R, C, L → More delay (RC), crosstalk, IR drop

3. Wire Design Rules (Typical)

Rule	Description	Symbol	Min. Value
Minimum Width	Minimum allowed width of a wire		W_{min}
Minimum Spacing	Minimum spacing between two parallel wires (same net or different net)		S_{min}
End of Wire Enclosure	Wire must extend beyond via or contact by minimum enclosure		E_{min}
Wire to Active/Poly Spacing	Spacing between wire and active/poly region		$S_{wa,min}$
Corner / Bend Spacing	Spacing at 90° corners to avoid etch issues		$S_{corner,min}$

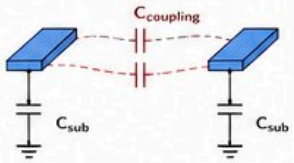
4. Via Design Rules (Typical)

Rule	Description	Symbol	Min. Value
Via Size	Minimum via (cut) size		$V_{min} \times V_{min}$
Via to Via Spacing	Spacing between two vias (same layer)		$S_{v,min}$
Via Enclosure	Minimum metal overlap around via		$E_{x,min}$, $E_{y,min}$
Via to Wire Spacing	Spacing between via and wire		$S_{vw,min}$
Stacked Via Alignment	Vias in two adjacent layers should be aligned within tolerance		Δ_{align}

5. Common Parasitic Sources in Layout

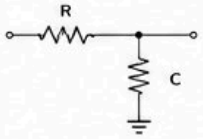
(a) Interconnect Parasitics

- Wire Resistance (R)
- Wire Capacitance (C)
  - To substrate
  - To adjacent wires (coupling)
- Wire Inductance (L)



(b) Parasitic Effects

- Increased delay
- Crosstalk noise
- Higher dynamic power
- IR drop and electromigration



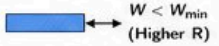
Distributed RC model of a long wire

6. Typical Layout Examples

(a) Wide vs Thin Wire

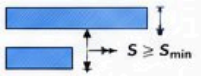
Preferred

Not Preferred

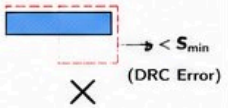


(b) Proper Spacing

Correct



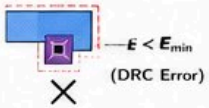
Incorrect



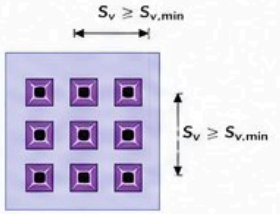
(c) Wire Enclosure over Via

Correct

Incorrect

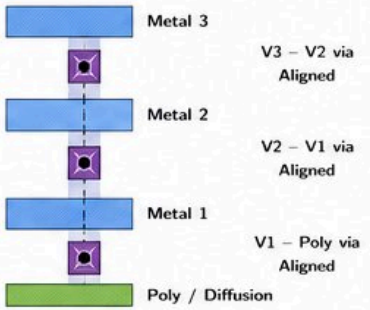


(d) Via Array (Good Layout)



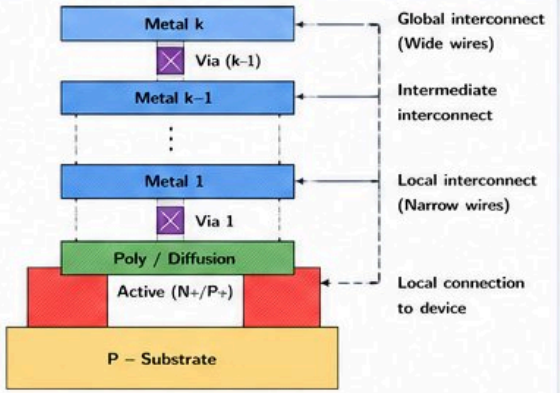
Use via arrays for low resistance in power/ground nets.

7. Via Stack Example



Misalignment > Δ_{align} → DRC Error and reliability issues.

8. Wire Layers and Cross-Section



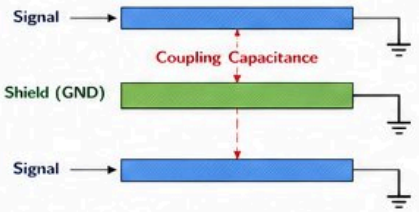
9. Design Rule Summary (Example Technology: 65nm)

Parameter	Symbol	Min. Value	Unit
Minimum Metal 1 Width	W_{M1}	0.14	μm
Minimum Metal 2 Width	W_{M2}	0.14	μm
Minimum Spacing (M1–M1)	S_{M1}	0.14	μm
Minimum Spacing (M1–M2)	S_{12}	0.14	μm
Via1 Size (Cut)	V_1	0.08 × 0.08	μm
Via1 Enclosure (M1)	E_{M1}	0.06	μm
Via1 Enclosure (Poly/Diff)	E_P	0.06	μm
Via1 to Via1 Spacing	S_{V1}	0.14	μm
Metal1 to Active Spacing	S_{MA}	0.14	μm

Note: Values are technology dependent. Always refer to foundry PDK.

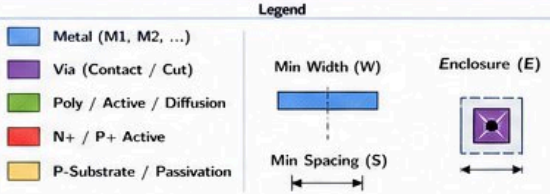
10. Parasitic Reduction Guidelines

- ✓ Use wider wires for critical nets (lower R).
- ✓ Use minimum length and metal layers wisely.
- ✓ Maintain proper spacing to reduce crosstalk.
- ✓ Use via arrays for power/ground nets.
- ✓ Follow design rules strictly.
- ✓ Shield sensitive nets with ground wires.
- ✓ Use metal fill / dummy structures as per DRC rules.



11. Key Takeaways

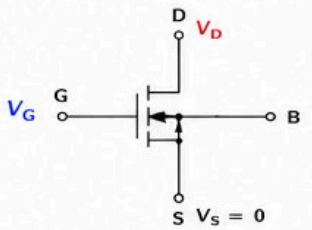
- ✓ Parasitic R, C, L of interconnects impact circuit performance.
- ✓ Wires and vias must follow min width, spacing, enclosure and alignment rules.
- ✓ Use proper via stacks and arrays for low resistance.
- ✓ Good layout reduces delay, noise, power and improves yield.
- ✓ Always run DRC and LVS before tape-out.



SPICE SIMULATION OF MOSFET I–V CHARACTERISTICS

1. MOSFET UNDER TEST

NMOS Enhancement Device
(Example: Level–1 Model)



Device Parameters

V_{TO}	= 0.7 V
K_P	= 200 μA/V^2
λ	= 0.02 V^{-1}
W/L	= 10 μm / 1 μm

2. SPICE NETLIST (Ngspice / LTspice)

```
* NMOS I–V Characteristics
M1 D G 0 0 NMOS1 W=10u L=1u
VDD D 0 DC 10
VGG G 0 DC 0
.model NMOS1 NMOS (
+ LEVEL=1 VTO=0.7 KP=200e-6 LAMBDA=0.02
+ GAMMA=0.0 PHI=0.6 )
.op
.control
* Sweep VDS for different VGS
let vgslist = 0 0.8 1.2 1.6 2.0 2.5 3.0 4.0 5.0
foreach vgs $vgslist
  alter VGG $vgs
  dc VDD 0 10 0.01
  wrdata Id_Vds_@vgs@.dat V(DD) -I(VDD)
end
.endc
.end
```

Id = –I(VDD)
Vds = V(DD)

3. SIMULATION SETUP

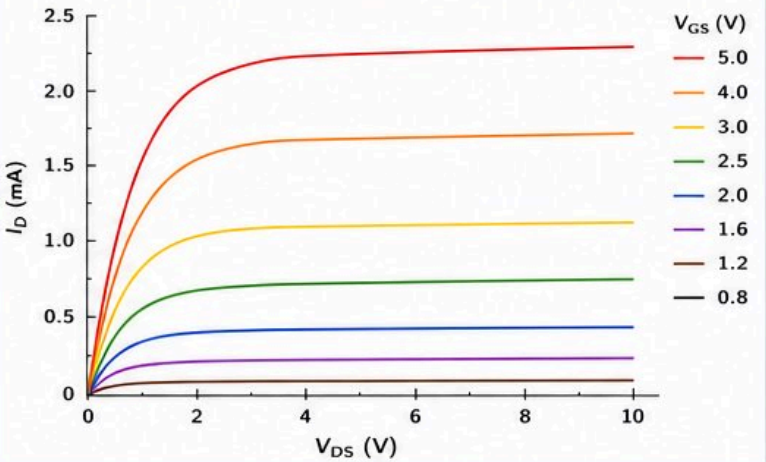
DC Sweep : $V_{DS} = 0 \rightarrow 10$ V
(Step = 0.01 V)

For each V_{GS}
V_{GS} = 0, 0.8, 1.2, 1.6,
2.0, 2.5, 3.0, 4.0, 5.0 V

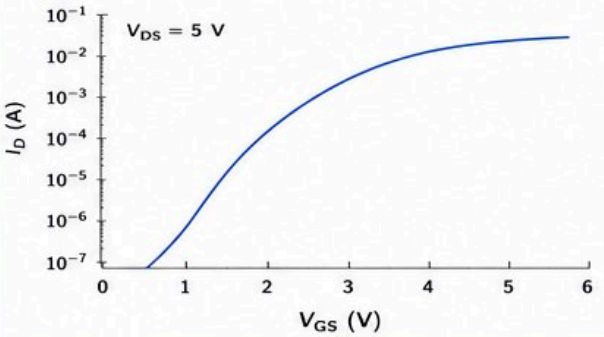
Plot:
1. I_D vs V_{DS} (Output Characteristics) for various V_{GS}
2. I_D vs V_{GS} (Transfer Characteristic) at fixed V_{DS} (e.g., V_{DS} = 5 V)

Run in Ngspice:
`ngspice mos_iv.cir`

4. OUTPUT CHARACTERISTICS (I_D vs V_{DS})



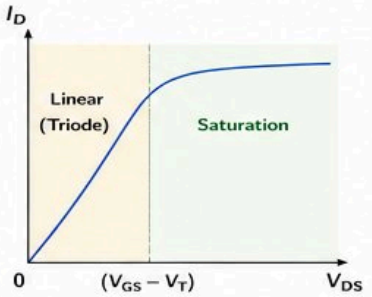
5. TRANSFER CHARACTERISTIC (I_D vs V_{GS})



6. REGIONS OF OPERATION (from I_D–V_{DS} curves)

For a given V_{GS}:

- Linear (Triode) Region:
  $0 \le V_{DS} < (V_{GS} - V_T)$
  I_D increases almost linearly with V_{DS}.
- Saturation Region:
  $V_{DS} \ge (V_{GS} - V_T)$
  I_D ~ constant
  (slight slope due to λ).

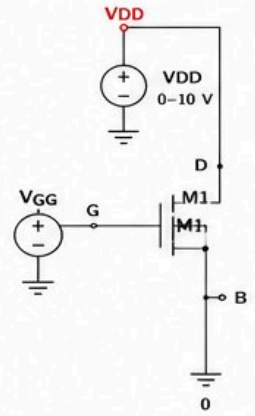


7. EXTRACTED PARAMETERS (Example from Simulation)

Parameter	Method	Example Value
V_T (Threshold Voltage)	Extrapolate $I_D^{1/2}$–V_{GS}	≈ 0.70 V
K_P (Transconductance Parameter)	From slope of I_D in Linear Region	≈ 200 μA/V^2
λ (Channel Length Modulation)	From slope in Saturation: $I_D = I_{D0}(1 + \lambda V_{DS})$	≈ 0.02 V^{-1}
g_m (Transconductance)	$dI_D/dV_{GS}\,\vert_{V_{DS}=5V}$	≈ 1.2 mS @ V_{GS}=2.5 V
I_{ON}	I_D at V_{GS}=5V, V_{DS}=5V	≈ 2.1 mA

(Values depend on model and W/L used)

8. COMPLETE SPICE EXAMPLE (Ngspice)

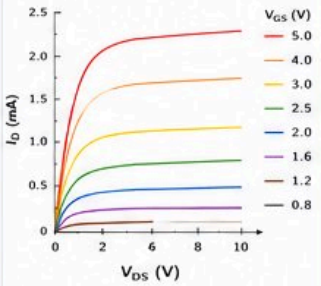



```
* MOSFET I–V Simulation
M1 D G 0 0 NMOS1 W=10u L=1u
VDD D 0 DC 10
VGG G 0 DC 0
.model NMOS1 NMOS (LEVEL=1 VTO=0.7 KP=200e-6 LAMBDA=0.02)
.control
let vgslist = 0 0.8 1.2 1.6 2.0 2.5 3.0 4.0 5.0
foreach vgs $vgslist
  alter VGG $vgs
  dc VDD 0 10 0.01
  plot -I(VDD) vs V(DD) title 'VGS = $vgs V'
end
let vds5 = @VDD[500] * at VDS = 5V (index 500 for 0–10V, step=0.01)
foreach vgs $vgslist
  alter VGG $vgs
  op
  print -I(VDD) $vds5
end
.endc
.end
```

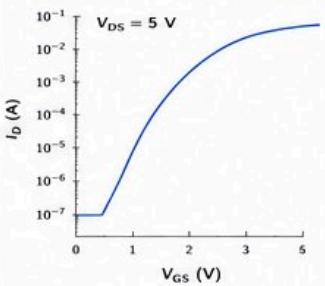
- -I(VDD) gives I_D
- V(DD) gives V_{DS}

9. HOW TO OBTAIN PLOTS

(a) Output Characteristics
Run the control block.
It plots I_D–V_{DS} for each V_{GS}.



(b) Transfer Characteristic
Use saved data at V_{DS} = 5 V.
Plot I_D vs V_{GS} (semi-log scale).



10. KEY TAKEAWAYS

- ✓ SPICE accurately predicts MOSFET I–V characteristics.
- ✓ Output curves show linear and saturation regions.
- ✓ Transfer curve in log scale helps find V_T.
- ✓ Design parameters (V_T, K_P, λ, g_m) can be extracted.
- ✓ Change W/L, model parameters and rerun simulation to study their effects.

Useful Commands (Ngspice / LTspice)

DC Sweep	: dc V_sounce start stop step
OP Point	: op
Plot	: plot –I(VDD) vs V(DD)
Print Value	: print –I(VDD) V(DD)

MOSFET PARAMETERS EXTRACTION – FROM IV CURVES

1. Introduction

- SPICE models require accurate device parameters (V_T, K_P, λ, etc.).
- These parameters can be extracted from simulated or measured $I-V$ characteristics.

Example Device

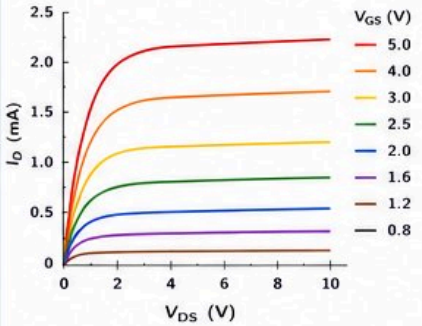
NMOS (Level–1 Model)

$W = 10\ \mu m$ $L = 1\ \mu m$

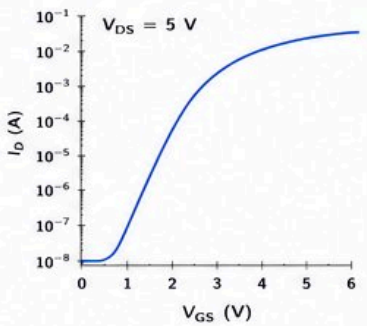
(Values used in simulation for illustration)

2. IV Curves Used

(a) Output Characteristics
I_D vs V_{DS} (for various V_{GS})



(b) Transfer Characteristics
I_D vs V_{GS} (at fixed V_{DS})



3. Parameters to Be Extracted

- V_T : Threshold Voltage (V)
- K_P : Transconductance Parameter (A/V^2)
- λ : Channel Length Modulation (1/V)
- I_{ON} : Drain Current in Saturation (at given bias)

Level–1 Model Equations

Triode Region ($0 < V_{DS} < V_{GS} - V_T$)

$$I_D = K_P \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Saturation Region ($V_{DS} \geq V_{GS} - V_T$)

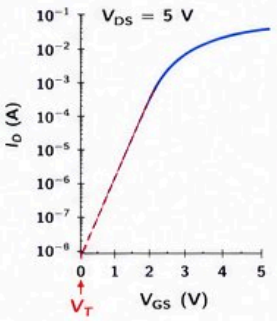
$$I_D = \frac{K_P}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

where $K_P = \mu_n C_{ox} \frac{W}{L}$

4. Extraction of V_T (Threshold Voltage)

Method: Linear Extrapolation from Transfer Curve (in Subthershold to Weak Inversion Region)

1. Plot I_D vs V_{GS} (log scale).
2. In the moderate inversion region, the curve is approximately linear.
3. Extrapolate the linear portion to intersect the V_{GS} axis at $I_D = 10^{-7}$ A (or $I_D = 0$ for strong inversion).



From the plot (example):

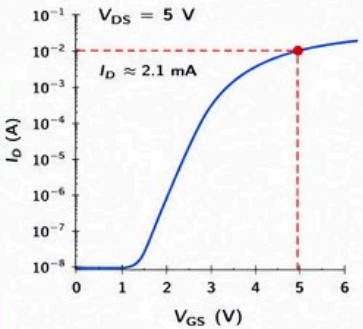
$V_T \approx 0.65$ V

5. Extraction of K_P (Transconductance Parameter)

Method: Using Saturation Region Equation (at a fixed $V_{DS} >> V_{GS} - V_T$)

1. From transfer curve, take a point in saturation region (e.g., $V_{GS} = 5$V, $V_{DS} = 5$V).
2. Use $I_D = \frac{K_P}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$

   If λ is small, $(1 + \lambda V_{DS}) \approx 1$.



Example:

At $V_{GS} = 5$V, $V_{DS} = 5$V, from plot $I_D \approx 2.1$ mA

$V_T = 0.65$ V (from previous step)

$$K_P = \frac{2 I_D}{(V_{GS} - V_T)^2} = \frac{2(2.1 \times 10^{-3})}{(5 - 0.65)^2}$$

$$K_P \approx 2.22 \times 10^{-4}\ \text{A/V}^2 = 222\ \mu\text{A/V}^2$$

6. Extraction of λ (Channel Length Modulation)

Method: From Output Characteristics in Saturation Region (at constant V_{GS})

In saturation, $I_D = I_{D0}(1 + \lambda V_{DS})$

$\Rightarrow$ Plot I_D vs V_{DS}, slope gives λ.

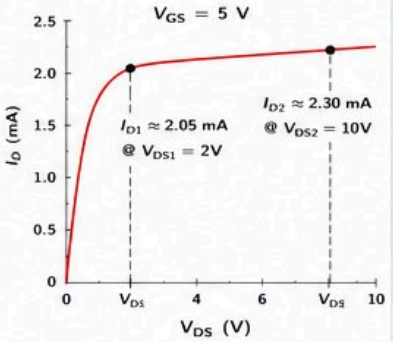
Example (Using $V_{GS} = 5$ V Curve):

From the plot:

At $V_{DS1} = 2$V, $I_{D1} \approx 2.05$ mA

At $V_{DS2} = 10$V, $I_{D2} \approx 2.30$ mA

$$\lambda = \frac{I_{D2} - I_{D1}}{I_{D1}(V_{DS2} - V_{DS1})} = \frac{2.30 - 2.05}{(2.05)(10 - 2)} \approx 0.0152\ \text{V}^{-1}$$



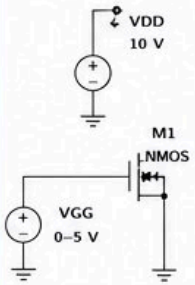
7. Summary of Extracted Parameters

Parameter	Symbol	Extracted Value (Example)	Unit
Threshold Voltage	V_T	0.65	V
Transconductance Parameter	K_P	222	μA/V^2
Channel Length Modulation	λ	0.0152	V^{-1}
I_D at V_{GS}=5V, V_{DS}=5V	I_{ON}	2.1	mA

These parameters can be used in Level–1 SPICE model:

```
.model NMOS1 NMOS (
+ LEVEL=1 VTO=0.65 KP=222e-6 LAMBDA=0.0152
+ GAMMA=0 PHI=0.6 )
```

8. Complete Spice Example

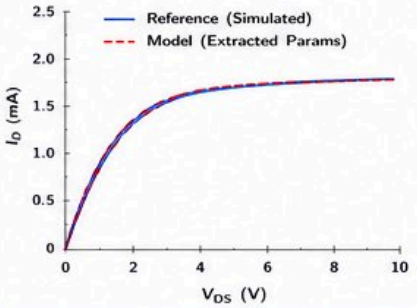



```
* MOSFET Parameter Extraction Example
VDD  D  0  DC  10
VGG  G  0  DC  0
M1   D  G  0  0  NMOS1  W=10u  L=1u
.model NMOS1 NMOS (LEVEL=1 VTO=0.65 KP=222e-6 LAMBDA=0.0152
+ GAMMA=0 PHI=0.6 )
.op
* Sweep VDS for different VGS
.dc VDD  0  10  0.01
.step param vg  0.8  5  0.6
alter  VGG  $vg
.end
```

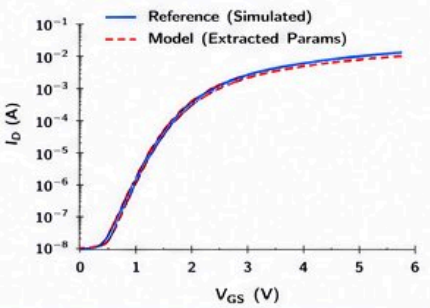
This will generate $I_D - V_{DS}$ and $I_D - V_{GS}$ characteristics.

9. Validation (Model vs Reference Curves)

(a) Output Characteristics ($V_{GS} = 5$V)



(b) Transfer Characteristics ($V_{DS} = 5$V)



Good overlap indicates accurate extraction.
Small deviations may occur due to measurement/simulation noise and model simplifications.

10. Key Takeaways

- ✓ V_T extracted from transfer curve (linear extrapolation).
- ✓ K_P extracted from saturation current using $I_D = \frac{K_P}{2}(V_{GS} - V_T)^2$.
- ✓ λ extracted from slope of I_D vs V_{DS} in saturation.
- ✓ Extracted parameters allow accurate SPICE modeling and design prediction.
- ✓ Repeat extraction for different W/L, temperature, or technology for best accuracy.

Tips

- Use long-channel devices for Level–1 extraction.
- Ensure V_{DS} is large enough for saturation.
- Use log scale for transfer curve to clearly see V_T.